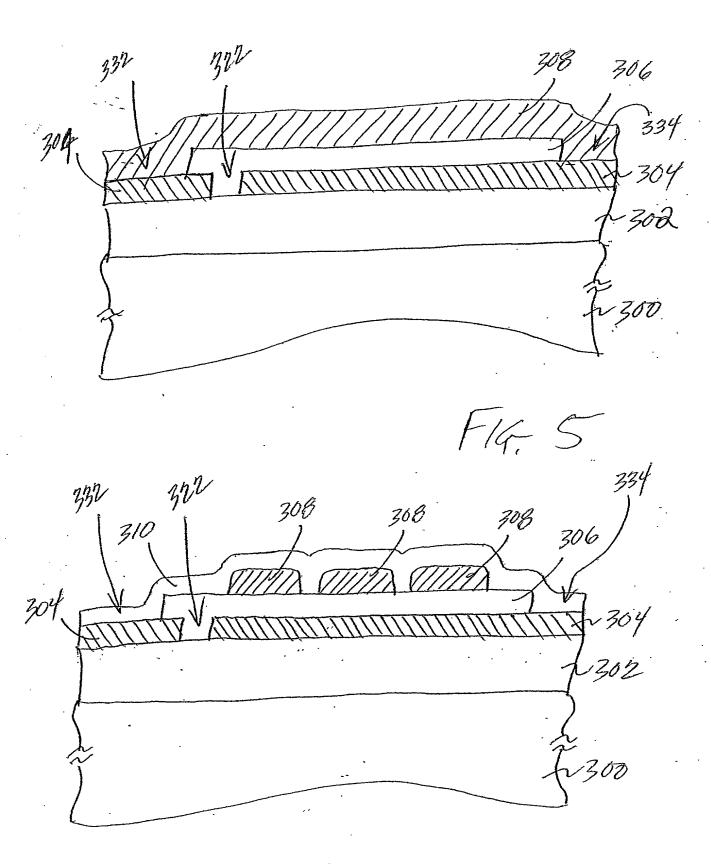


FORM FIRST DIELECTRIC LAYER OVER SEMICONDUCTOR SUBSTRATE W 202		
FORM FIRST MAGNETIC LAYER OVER FIRST DIELECTRIC LAYER		
V		
PATTERN FIRST MAGNETIC LAYER TO DEFINE AT LEAST ONE SLOT		
V		
FORM SECOND DIELECTRIC LAYER OVER FIRST MAGNETIC LAYER, FILLING EACH SLOT IN FIRST MAGNETIC LAYER		
PATTERN SECOND DIELECTRIC LAYER TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER		
FORM CONDUCTIVE LAYER OVER SECOND DIELECTRIC LAYER W2/2		
PATTERN CONDUCTIVE LAYER TO FORM A CONDUCTOR HAVING A SPIRAL-SHAPED SIGNAL PATH AND TO CLEAR ANY VIAS TO FIRST MAGNETIC LAYER		
V		
FORM THIRD DIELECTRIC LAYER OVER CONDUCTIVE LAYER JU 216		
V		
PATTERN THIRD DIELECTRIC LAYER TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER		
·		
FORM SECOND MAGNETIC LAYER OVER THIRD DIELECTRIC LAYER, FILLING ANY VIAS TO FIRST MAGNETIC LAYER		
PATTERN SECOND MAGNETIC LAYER TO FORM AT LEAST ONE SLOT		

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İ	FORM UNDERLYING LAYER OVER DIELECTRIC LAYER	NBOL
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FORM MAGNETIC MATERIAL LAYER OVER UNDERLYING LAYER

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FORM OVERLYING LAYER OVER MAGNETIC MATERIAL LAYER

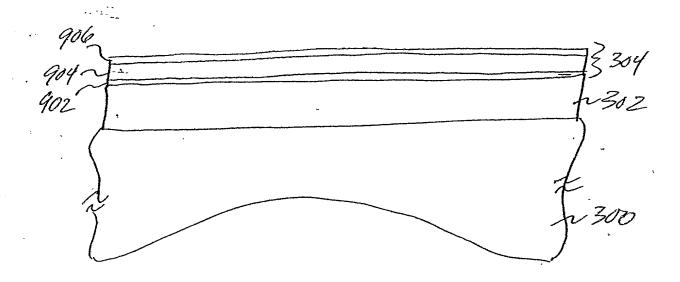
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FORM PATTERNED MASK LAYER OVER OVERLYING LAYER

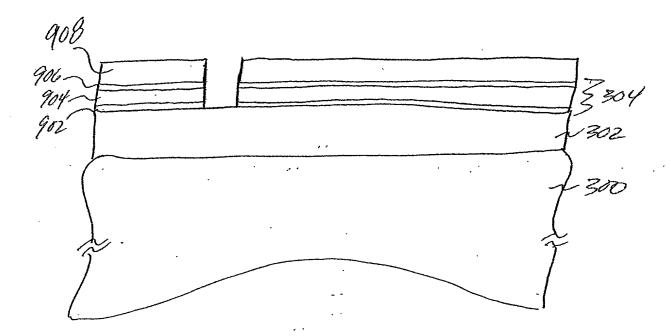
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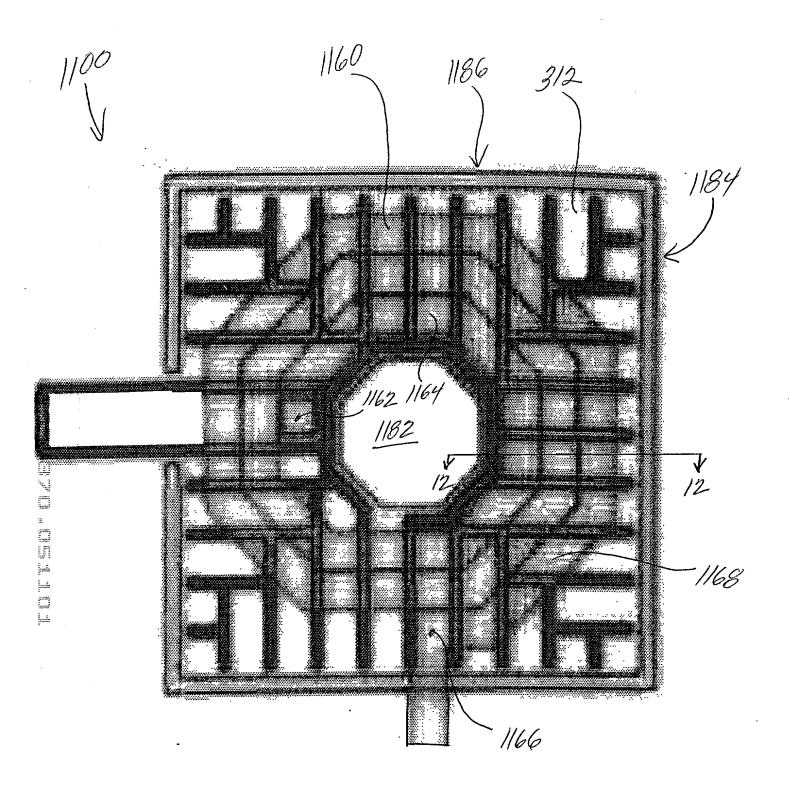
ETCH UNDERLYING, MAGNETIC MATERIAL, AND OVERLYING LAYERS

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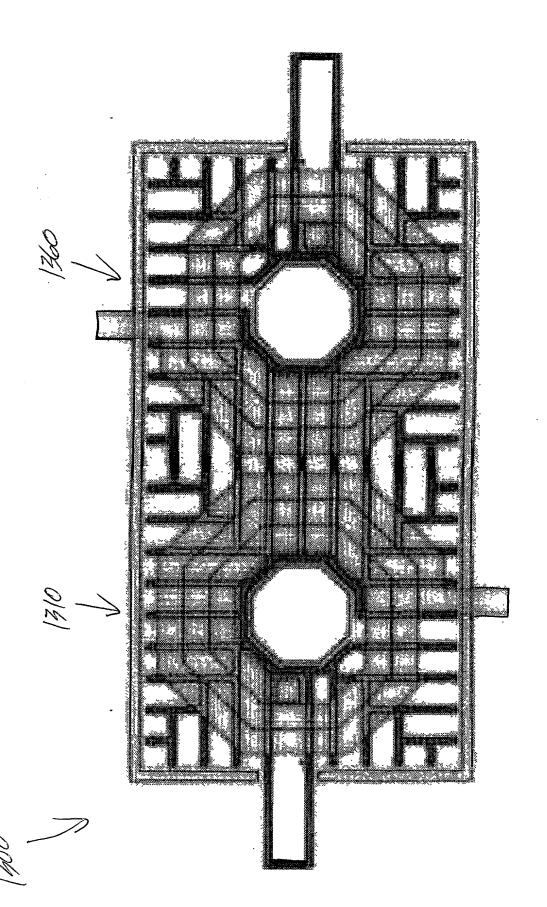




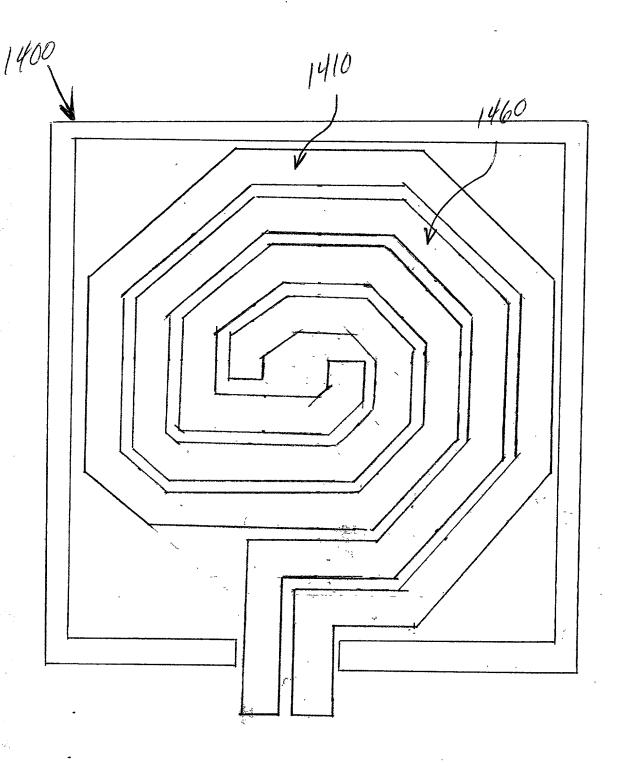


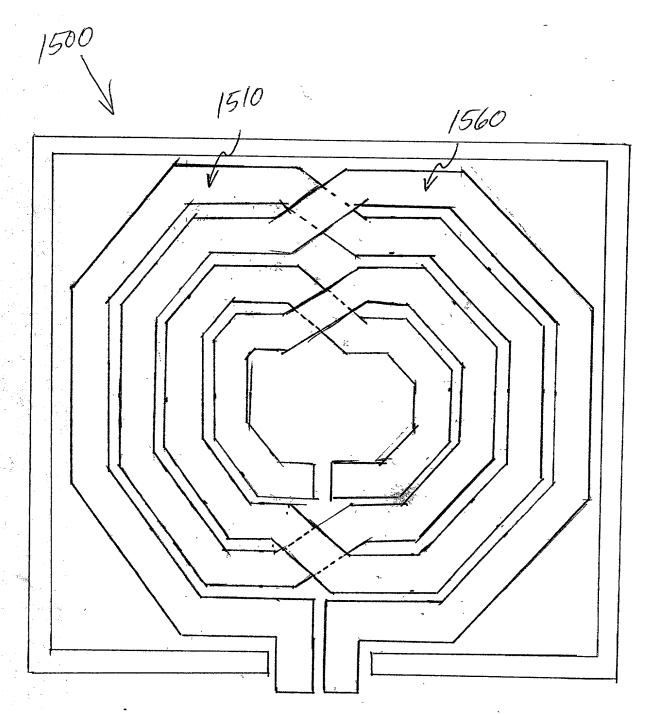
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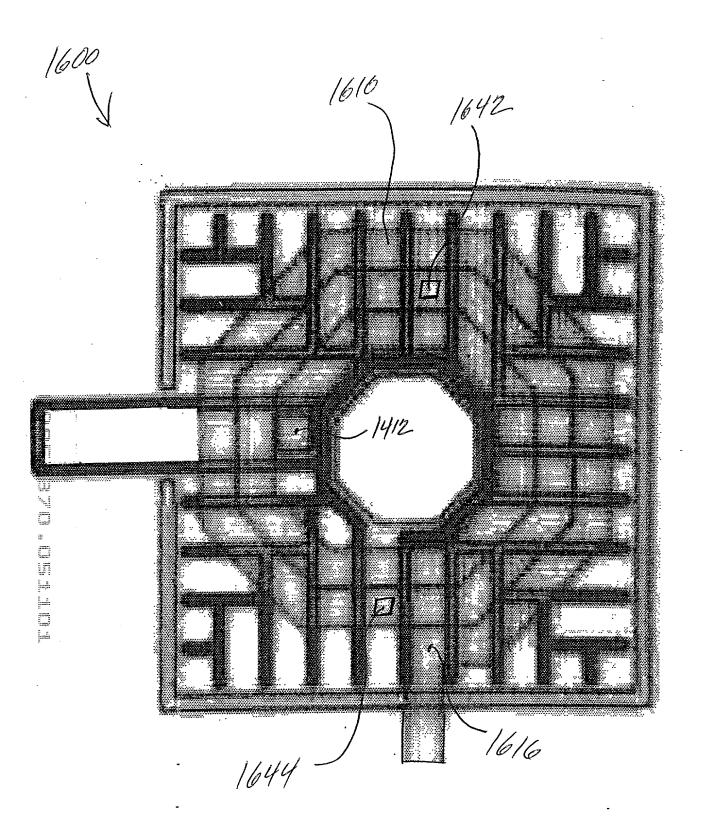
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